Ashly Word Clock Inputs and Outputs.

A word clock signal is typically a 0 to 5V square wave at the digital audio sampling rate. The word clock jacks use standard 75 ohm BNC connectors, and standard 75 ohm coaxial cable should be used (coaxial television cable, not shielded mic cable).

There is no official AES standard mandating what a word clock signal must be, but there is a "recommended practice" for word clock as a part of AES11. The audio industry has generally settled on a 0 to 5V square wave where the left channel corresponds to the word clock being high and the right channel is when the word clock is low. Note for our test technicians that this left=high/right=low convention is opposite of the convention used for the Philips I2S digital audio left/right clocks used *inside* our products.

You may encounter word clock signals that are only 3.3V or 2.4V from other manufacturers, and they may be DC or AC coupled giving –1.2V to +1.2V. Ashly's word clock *input* can operate from 1Vpp to 7Vpp, AC or DC coupled. Ashly's word clock *output* is DC coupled 0 to 5V when unterminated.

Word clock lines should have a 75 ohm source impedance and a 75 ohm load termination at the farthest end of the line. Without these line terminations, the quality of the word clock degrades significantly over long distance (hundreds of feet) and may cause a loss of PLL lock in the receiving equipment. Over short lines (say between equipment racks in the same room) these terminations are recommended, but not absolutely necessary.

The word clock switch on Ashly equipment provides two functions. First, it routes the word clock input signal hard-wired looped-through to the word clock output jack when in the OUT position (marked "loop" on the back panel), but breaks the signal and generates an internal word clock source in the IN position (marked "term" on the back panel). Secondly, the OUT position does not apply any load to the looped-through word clock signal, but the IN position applies a 75 ohm termination to the word clock input and supplies a 75 ohm source impedance to the word clock output. Therefore, the word clock switch should be in the IN "term" position whenever the unit is at either end of the word clock line, and in the OUT "loop" position when placed anywhere along the line. No external terminations are ever needed on our processors.

Common questions:

When would someone need to use word clocks? There are two general cases that I could think of where one would need a word clock.

First, if two pieces of digital audio gear need to be synchronized, i.e. their sample rates are very slightly different and must be made to match exactly. This could happen if our processor is connected to a Cobranet network, but someone wants to feed an AES/EBU digital audio signal in from some other piece of gear not connected to the Cobranet. In this case, there are two different digital clock domains having slightly different sample rates like 48,000 Hz and 48,010 Hz which would case sample skipping.

The second general case where word clocks would be useful is when several pieces of gear are cascaded in an AES/EBU digital audio chain. Each digital audio input adds some small

amount of clocking jitter and perhaps sample delay. After several units, the accumulative jitter could cause a loss of lock (and hence loss of audio), increased distortion due to large amounts of jitter, or even a small delay. By connecting word clock to each device, they all become precisely synchronized to the word clock master.

I see indicators on the front of the ne8800 processor for four different Clock Sources. What do I need to know about this and how should I configure this? The processor defaults to "Auto Selection" where the processor will automatically detect a Network, Word Clock, AES/EBU, or Internal master clock source and automatically switch, in this order of priority. Therefore, in most system configurations, the user doesn't need to worry about the master clock source, the processor will automatically pick the best master clock from the highest priority available. The processor will mute all audio outputs for about one second when it switches master clock sources. This Auto Selection mode can be over-riden in the control software by clicking on Device Options, Sample Rate & Master Clock Selection.

Why does the Network clock master have higher priority over a Word Clock master? In an ideal world, the word clock would always have the highest priority. Unfortunately, Cobranet on the Cirrus Logic CM2 board cannot slave-sync to a word clock or any other external master clock source; therefore, Cobranet must always be the highest priority clock source.

Does Ashly's word clock circuit use a crystal-based phase locked loop for extremely low jitter? No. While crystal-based PLL's do give very low jitter noise, our PLL is not based on a crystal because crystal-based PLL's have a very narrow lock range (only about +/-10Hz), so loss of lock and hence loss of audio would be a common problem. Even though the internal word clock PLL of Ashly equipment has a fairly large frequency lock range, the valid range has been intentionally limited to about 48KHz and 96KHz +/-4% so that a gross error in word clock sample rate does not cause gross errors in the DSP digital filters or DSP over-capacity utilization.